	Document ID	U	Title	Current OR
67	US 5212777 A	☒	Multi-processor reconfigurable in single instruction multiple data (SIMD) and multiple instruction multiple data (MIMD) modes and method of operation	712/229
68	US 5197140 A	☒	Sliced addressing multi-processor and method of operation	711/220
69	US 5185872 A	☒	System for executing different cycle instructions by selectively bypassing scoreboard register and canceling the execution of conditionally issued instruction if needed resources are busy	712/217
70	US 5043870 A	☒	Computer with automatic mapping of memory contents into machine registers during program execution	711/132
71	US 4926371 A	☒	Two's complement multiplication with a sign magnitude multiplier	708/628
72	US 4791550 A	☒	Higher order language-directed computer	709/106
73	US 4525780 A	☒	Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information	711/163
74	US 4507731 A	☒	Bidirectional data byte aligner	711/201
75	US 4493027 A	☒	Method of performing a call operation in a digital data processing system having microcode call and return operations	712/228
76	US 4455602 A	☒	Digital data processing system having an I/O means using unique address providing and access priority control techniques	710/5
77	US 4445177 A	☒	Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions	712/245
78	US 3858183 A	☐	DATA PROCESSING SYSTEM AND METHOD THEREFOR	711/118

	Document ID	U	Title	Current OR
44	US 5859991 A	☒	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
45	US 5854921 A	☒	Stride-based data address prediction structure	712/239
46	US 5826071 A	☒	Parallel mask decoder and method for generating said mask	712/224
47	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
48	US 5809288 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch on memory access stall	709/400
49	US 5784634 A	☒	Pipelined CPU with instruction fetch, execution and write back stages	712/1
50	US 5781789 A	☒	Superscaler microprocessor employing a parallel mask decoder	712/23
51	US 5768609 A	☒	Reduced area of crossbar and method of operation	712/11
52	US 5761469 A	☒	Method and apparatus for optimizing signed and unsigned load processing in a pipelined processor	712/210
53	US 5758195 A	☒	Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register	712/300
54	US 5752069 A	☒	Superscalar microprocessor employing away prediction structure	712/23
55	US 5696913 A	☒	Unique processor identifier in a multi-processing system having plural memories with a unified address space corresponding to each processor	710/317
56	US 5673396 A	☒	Adjustable depth/width FIFO buffer for variable width data transfers	710/307
57	US 5659785 A	☒	Array processor communication architecture with broadcast processor instructions	712/11
58	US 5638312 A	☒	Method and apparatus for generating a zero bit status flag in a microprocessor	708/525
59	US 5606520 A	☒	Address generator with controllable modulo power of two addressing capability	708/491
60	US 5592405 A	☒	Multiple operations employing divided arithmetic logic unit and multiple flags register	708/518
61	US 5522083 A	☒	Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors	712/22
62	US 5495433 A	☒	Data processing circuit	708/490
63	US 5410649 A	☒	Imaging computer system and network	345/505
64	US 5339447 A	☒	Ones counting circuit, utilizing a matrix of interconnected half-adders, for counting the number of ones in a binary string of image data	377/82
65	US 5282153 A	☒	Arithmetic logic unit	708/233
66	US 5253195 A	☒	High speed multiplier	708/627

	Document ID	U	Title	Current OR
21	US 6094711 A	☒	Apparatus and method for reducing data bus pin count of an interface while substantially maintaining performance	711/169
22	US 6070003 A	☒	System and method of memory access in apparatus having plural processors and plural memories	710/317
23	US 6041387 A	☒	Apparatus for read/write-access to registers having register file architecture in a central processing unit	711/5
24	US 6038584 A	☒	Synchronized MIMD multi-processing system and method of operation	709/248
25	US 6023776 A	☒	Central processing unit having a register which store values to vary wait cycles	714/55
26	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
27	US 5987561 A	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
28	US 5978907 A	☒	Delayed update register for an array	712/239
29	US 5935239 A	☒	Parallel mask decoder and method for generating said mask	712/224
30	US 5933624 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors while one processor services an interrupt	709/400
31	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
32	US 5924114 A	☒	Circular buffer with two different step sizes	711/110
33	US 5903486 A	☒	Device for digitally carrying out a division operation	708/655
34	US 5901001 A	☒	Data processor and method of processing data	712/212
35	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
36	US 5889948 A	☒	Apparatus and method for inserting an address in a data stream through a FIFO buffer	709/213
37	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
38	US 5881272 A	☒	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors on write to program counter of one processor	709/400
39	US 5878255 A	☒	Update unit for providing a delayed update to a branch prediction array	712/240
40	US 5875324 A	☒	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
41	US 5875315 A	☒	Parallel and scalable instruction scanning unit	712/204
42	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
43	US 5860104 A	☒	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137

	Document ID	U	Title	Current OR
1	US 20030 06992 0 A1	☐	Multi-threaded packet processing engine for stateful packet processing	709/108
2	US 20030 06147 1 A1	☒	Data processor	712/226
3	US 20030 05606 4 A1	☒	Method and apparatus for aligning memory write data in a microprocessor	711/154
4	US 20020 16603 7 A1	☒	Memory processing in a microprocessor	711/201
5	US 20020 13369 2 A1	☒	Data processor	712/244
6	US 20020 12083 0 A1	☒	Data processor assigning the same operation code to multiple operations	712/209
7	US 20020 05603 8 A1	☒	Data processor	712/241
8	US 20010 05503 2 A1	☒	Data processing method, recording medium and data processing apparatus	345/660
9	US 65671 82 B1	☒	Scan conversion of polygons for printing file in a page description language	358/1.15
10	US 65606 97 B2	☒	Data processor having repeat instruction processing using executed instruction number counter	712/245
11	US 64842 53 B1	☒	Data processor	712/212
12	US 63538 43 B1	☒	High performance universal multiplier circuit	708/631
13	US 63453 57 B1	☒	Versatile branch-less sequence control of instruction stream containing step repeat loop block using executed instructions number counter	712/241
14	US 63381 35 B1	☒	Data processing system and method for performing an arithmetic operation on a plurality of signed data values	712/221
15	US 62887 24 B1	☒	Clipping and trapezoid decomposition of polygons for printing files in a page description language	345/621
16	US 62826 33 B1	☒	High data density RISC processor	712/208
17	US 62694 36 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
18	US 62600 88 B1	☒	Single integrated circuit embodying a risc processor and a digital signal processor	710/100
19	US 62335 97 B1	☒	Computing apparatus for double-precision multiplication	708/625
20	US 61890 68 B1	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3

	Document ID	U	Title	Current OR
44	US 5512896 A	☒	Huffman encoding method, circuit and system employing most significant bit change for size detection	341/65
45	US 5509129 A	☒	Long instruction word controlling plural independent processor operations	712/203
46	US 5493524 A	☒	Three input arithmetic logic unit employing carry propagate logic	708/709
47	US 5485411 A	☒	Three input arithmetic logic unit forming the sum of a first input anded with a first boolean combination of a second input and a third input plus a second boolean combination of the second and third inputs	708/230
48	US 5479166 A	☒	Huffman decoding method, circuit and system employing conditional subtraction for conversion of negative numbers	341/65
49	US 5471593 A	☒	Computer processor with an efficient means of executing many instructions simultaneously	712/235
50	US 5465224 A	☒	Three input arithmetic logic unit forming the sum of a first Boolean combination of first, second and third inputs plus a second Boolean combination of first, second and third inputs	708/236
51	US 5446651 A	☒	Split multiply operation	708/630
52	US 5442581 A	☒	Iterative division apparatus, system and method forming plural quotient bits per iteration	708/653
53	US 5420809 A	☒	Method of operating a data processing apparatus to compute correlation	708/200
54	US 4495598 A	☒	Computer rotate function	712/300
55	US 4488252 A	☒	Floating point addition architecture	708/505
56	US 4149263 A	☒	Programmable multi-bit shifter	377/69
57	US 4135242 A	☐	Method and processor having bit-addressable scratch pad memory	712/245

	Document ID	U	Title	Current OR
22	US 5805913 A	☒	Arithmetic logic unit with conditional register source selection	712/209
23	US 5761726 A	☒	Base address generation in a multi-processing system having plural memories with a unified address space corresponding to each processor	711/147
24	US 5742538 A	☒	Long instruction word controlling plural independent processor operations	708/620
25	US 5734880 A	☒	Hardware branching employing loop control registers loaded according to status of sections of an arithmetic logic unit divided into a plurality of sections	712/221
26	US 5727225 A	☒	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/224
27	US 5712999 A	☒	Address generator employing selective merge of two independent addresses	711/211
28	US 5696959 A	☒	Memory store from a selected one of a register pair conditional upon the state of a selected status bit	712/245
29	US 5696954 A	☒	Three input arithmetic logic unit with shifting means at one input forming a sum/difference of two inputs logically anded with a third input logically ored with the sum/difference logically anded with an inverse of the third input	712/221
30	US 5694348 A	☒	Method apparatus and system for correlation	708/525
31	US 5689695 A	☒	Conditional processor operation based upon result of two consecutive prior processor operations	712/234
32	US 5680339 A	☒	Method for rounding using redundant coded multiply result	708/493
33	US 5655096 A	☒	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
34	US 5644524 A	☒	Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive or	708/655
35	US 5644522 A	☒	Method, apparatus and system for multiply rounding using redundant coded multiply result	708/551
36	US 5640578 A	☒	Arithmetic logic unit having plural independent sections and register storing resultant indicator bit from every section	712/221
37	US 5634065 A	☒	Three input arithmetic logic unit with controllable shifter and mask generator	708/230
38	US 5606677 A	☒	Packed word pair multiply operation forming output including most significant bits of product and other bits of one input	712/208
39	US 5600847 A	☒	Three input arithmetic logic unit with mask generator	712/36
40	US 5596763 A	☒	Three input arithmetic logic unit forming mixed arithmetic and boolean combinations	708/670
41	US 5596519 A	☒	Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive OR	708/655
42	US 5590350 A	☒	Three input arithmetic logic unit with mask generator	712/36
43	US 5581720 A	☒	Perpetual calendar	40/114

	Document ID	U	Title	Current OR
1	US 20030108040 A1	☐	Banyan switched processor datapath	370/389
2	US 20030105793 A1	☒	Long instruction word controlling plural independent processor operations	708/625
3	US 20020111977 A1	☒	Hardware assist for data block diagonal mirror image transformation	708/400
4	US 20020108026 A1	☒	Data processing apparatus with register file bypass	712/218
5	US 6370558 B1	☒	Long instruction word controlling plural independent processor operations	708/603
6	US 6240437 B1	☒	Long instruction word controlling plural independent processor operations	708/524
7	US 6219688 B1	☒	Method, apparatus and system for sum of plural absolute differences	708/709
8	US 6173394 B1	☒	Instruction having bit field designating status bits protected from modification corresponding to arithmetic logic unit result	712/226
9	US 6173305 B1	☒	Division by iteration employing subtraction and conditional source selection of a prior difference or a left shifted remainder	708/650
10	US 6116768 A	☒	Three input arithmetic logic unit with barrel rotator	708/236
11	US 6098063 A	☒	Three input arithmetic logic unit with shifter	712/20
12	US 6067613 A	☒	Rotation register for orthogonal data transformation	712/32
13	US 6058473 A	☒	Memory store from a register pair conditional upon a selected status bit	712/225
14	US 6032170 A	☒	Long instruction word controlling plural independent processor operations	708/620
15	US 6026484 A	☒	Data processing apparatus, system and method for if, then, else operation using write priority	712/226
16	US 6016538 A	☒	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/32
17	US 5995748 A	☒	Three input arithmetic logic unit with shifter and/or mask generator	712/221
18	US 5995747 A	☒	Three input arithmetic logic unit capable of performing all possible three operand boolean operations with shifter and/or mask generator	712/221
19	US 5974539 A	☒	Three input arithmetic logic unit with shifter and mask generator	712/221
20	US 5961635 A	☒	Three input arithmetic logic unit with barrel rotator and mask generator	712/221
21	US 5960193 A	☒	Apparatus and system for sum of plural absolute differences	712/221

	L #	Hits	Search Text	DBs
1	L1	21444	(align$4 misalign$4) near10 (data operand)	USPAT; US-PGPUB
2	L2	3423	(extension extend$3) near5 sign	USPAT; US-PGPUB
3	L3	760	1 and 2	USPAT; US-PGPUB
4	L5	110	rotat$3 near20 2	USPAT; US-PGPUB
5	L8	5464	(align$4 misalign$4) near10 (data operand)	EPO; JPO; DERWENT; IBM_TDB
6	L9	532	(extension extend$3) near5 sign	EPO; JPO; DERWENT; IBM_TDB
7	L10	4	8 and 9	EPO; JPO; DERWENT; IBM_TDB
8	L6	57	1 and 5	USPAT; US-PGPUB
9	L7	78	1 near99 2 not 6	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
23	US 54993 80 A	☒	Data processor and read control circuit, write control circuit therefor	711/212
24	US 54816 89 A	☒	Conversion of internal processor register commands to I/O space addresses	711/202
25	US 54716 28 A	☒	Multi-function permutation switch for rotating and manipulating an order of bits of an input data byte in either cyclic or non-cyclic mode	712/223
26	US 54715 92 A	☒	Multi-processor with crossbar link of processors and memories and method of operation	709/213
27	US 53945 29 A	☒	Branch prediction unit for high-performance processor	712/240
28	US 53718 96 A	☒	Multi-processor having control over synchronization of processors in mind mode and method of operation	712/20
29	US 53394 19 A	☒	ANDF compiler using the HPcode-plus compiler intermediate language	717/147
30	US 53332 96 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171
31	US 53218 10 A	☒	Address method for computer graphics system	345/562
32	US 53177 20 A	☒	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
33	US 53156 98 A	☒	Method and apparatus for varying command length in a computer graphics system	345/522
34	US 52806 13 A	☒	ANDF installer using the HPcode-Plus compiler intermediate language	717/147
35	US 52768 81 A	☒	ANDF producer using the HPcode-Plus compiler intermediate language	717/147
36	US 52396 54 A	☒	Dual mode SIMD/MIMD processor providing reuse of MIMD instruction memories as data memories when operating in SIMD mode	712/20
37	US 52261 25 A	☒	Switch matrix having integrated crosspoint logic and method of operation	710/317
38	US 51558 43 A	☒	Error transition mode for multi-processor system	714/5
39	US 51465 92 A	☒	High speed image processing computer with overlapping windows-div	345/807
40	US 51290 60 A	☒	High speed image processing computer	345/563
41	US 51093 48 A	☒	High speed image processing computer	345/505
42	US 49858 48 A	☒	High speed image processing system using separate data processor and address generator	345/505
43	US 49550 24 A	☒	High speed image processing computer with error correction and logging	714/763
44	US 45690 16 A	☒	Mechanism for implementing one machine cycle executable mask and rotate instructions in a primitive instruction set computing system	712/224
45	US 43251 20 A	☒	Data processing system	711/202

	Document ID	U	Title	Current OR
1	US 20020 10802 7 A1	☐	Microprocessor and method of processing unaligned data in microprocessor	712/223
2	US 20020 07832 5 A1	☒	Microcomputer and dividing circuit	712/210
3	US 65394 70 B1	☒	Instruction decode unit producing instruction operand information in the order in which the operands are identified, and systems including same	712/208
4	US 65394 67 B1	☒	Microprocessor with non-aligned memory access	711/219
5	US 63433 57 B1	☒	Microcomputer and dividing circuit	712/210
6	US 62726 20 B1	☒	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
7	US 62533 08 B1	☒	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/210
8	US 62055 35 B1	☒	Branch instruction having different field lengths for unconditional and conditional displacements	712/33
9	US 61311 54 A	☒	Microcomputer having variable bit width area for displacement	712/32
10	US 61227 24 A	☒	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
11	US 60584 65 A	☒	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
12	US 59915 45 A	☒	Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word	712/33
13	US 59699 76 A	☒	Division circuit and the division method thereof	708/655
14	US 58389 84 A	☒	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
15	US 58318 77 A	☒	Bit searching through 8, 16, or 32 bit operands using a 32 bit data path	708/200
16	US 58093 20 A	☒	High-performance multi-processor having floating point unit	712/34
17	US 57544 60 A	☒	Method for performing signed division	708/653
18	US 56871 02 A	☒	Double precision (64 bit) shift operations using a 32 bit data path	708/209
19	US 56825 45 A	☒	Microcomputer having 16 bit fixed length instruction format	712/41
20	US 56823 39 A	☒	Method for performing rotate through carry using a 32 bit barrel shifter and counter	708/209
21	US 56551 39 A	☒	Execution unit architecture to support X86 instruction set and X86 segmented addressing	712/32
22	US 56131 46 A	☒	Reconfigurable SIMD/MIMD processor using switch matrix to allow access to a parameter memory by any of the plurality of processors	712/20

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1	L1	21444	(align$4 misalign$4) near10 (data operand)	USPAT; US-PGPUB
2	L2	3423	(extension extend$3) near5 sign	USPAT; US-PGPUB
3	L3	760	1 and 2	USPAT; US-PGPUB
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5	L8	5464	(align$4 misalign$4) near10 (data operand)	EPO; JPO; DERWENT; IBM_TDB
6	L9	532	(extension extend$3) near5 sign	EPO; JPO; DERWENT; IBM_TDB
7	L10	4	8 and 9	EPO; JPO; DERWENT; IBM_TDB
8	L6	57	1 and 5	USPAT; US-PGPUB
9	L7	78	1 near99 2 not 6	USPAT; US-PGPUB
10	L12	295	3 and rotat$3 not (6 7)	USPAT; US-PGPUB
11	L13	0	7 and 12	USPAT; US-PGPUB
12	L14	350882	(load$3 stor$3 boundary) near10 memory	USPAT; US-PGPUB
13	L15	1217	1 near99 14	USPAT; US-PGPUB
14	L21	45	15 and 12	USPAT; US-PGPUB